

Docket No. 500.42877X00  
Serial No. 10/600,771  
January 5, 2006

**AMENDMENTS TO THE SUBSTITUTE SPECIFICATION:**

**Page 35** – Please replace the paragraph beginning on line 9 and bridging to page 36, line 26, with the amended paragraph as follows:

The following solution was conceived. Since the embedding oxide film of the STI region is caused to fall from the silicon substrate, the side wall (namely, A portion of Fig. 5) of the trench becomes a free surface, so that the impurity-caused stress can be released and the STI stress can be reduced. Fig. 5 graphically represents an analysis as to an embedding oxide film fall-in amount (i.e., depth or recess amount) dependent characteristic of a stress which is produced on the silicon substrate surface in the case that after the STI structure has been formed, the impurity is implanted thereinto. This analysis is carried out under such a condition that the active width is 0.5  $\mu\text{m}$ ; the trench width of the STI structure is 0.3  $\mu\text{m}$ ; the depth of the trench is 0.35  $\mu\text{m}$ ; and the implanting depth of the impurity is 40 nm. An abscissa of Fig. 5 indicates a fall-in amount (symbol "B" of Fig. 5) of the embedding oxide film, and an ordinate of Fig. 5 indicates a stress which is produced on the surface of the silicon substrate. The stress which is produced on the silicon substrate surface is not so reduced in such a case that the fall-in amount (i.e., depth or recess amount) of the embedding oxide film is present within an impurity implanting region (namely, shorter than 40 nm of impurity implanting depth). However, when this fall-in amount of the embedding oxide film exceeds the impurity implanting region, this stress is rapidly reduced, and then this stress may become a substantially constant stress value when the fall-in amount of the embedding oxide film becomes an approximately half value of the trench depth, or shorter. The following fact can be revealed. That is, since the embedding oxide film of the STI region is caused to fall from the silicon substrate surface, the stress produced on the

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substrate surface can be reduced. Fig. 6 indicates such an experimental model that a transistor has been manufactured based upon this result. Fig. 6 shows a place which corresponds to the place of Fig. 2. Fig. 6 indicates such a result that while the transistor has been manufactured as the experimental model in accordance with the embodiment, the embedding oxide film was caused to fall by 50 nm from the substrate surface. It could become apparent that the crystalline defect occurring in Fig. 2 does not occur, and, therefore, this method of the present invention may become effective.

**Page 37** – Please replace the paragraph beginning on line 17 and bridging to page 38, line 8, with the amended paragraph as follows:

Also, as indicated in Fig. 5, it is preferable to make the fall-in amount of the embedding oxide film deeper than an implanting depth of an impurity in view of the stress reducing effect. In this specification, the expression "impurity implanting depth" implies such a value of " $R_p + \sigma$ " which is defined by adding standard deviation " $\sigma$ " of an impurity concentration fluctuation to a distance " $R_p$ ." This distance " $R_p$ " is defined from the surface of the silicon substrate up to an impurity peak concentration position of the impurity profile located in this silicon substrate. This impurity implanting depth corresponds to such a portion that a concentration depth becomes uniform at the position "C" of the manufacturing step of Fig. 1H. Since the peak concentration depths are largely changed in both the gate electrode edge portion and the element isolating portion edge portion, an impurity implanting depth may be measured in such a region having a shallow peak concentration depth, which is sandwiched by these edge portions.

**Page 55** – Please replace the paragraph beginning on line 16 and bridging to page 56, line 2, with the amended paragraph as follows:

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As the method of lowering the stress of the STI, there are two methods. In the first method, after the thermal oxide film 2 has been formed in the manufacturing step (1), the resulting substrate is thermally treated within NO gas, so that an oxynitride film is formed on both the bottom and side boundary surface planes at the interface between the silicon substrate and the two boundary planes of the thermal oxide film. Also, in the second method, the resulting substrate is exposed to nitrogen plasma so as to form an oxynitride film on the exposed two surfaces on the bottom and side surface planes of the thermal oxide film. These two reducing methods may suppress diffusion of oxygen so as to lower the STI stress, but cannot completely prevent this diffusion of oxygen. As a consequence, even in the case that these reducing methods are carried out, this method may become effective.